Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

Claim 1-121. (canceled)

122. (currently amended) A circuitry component comprising:

a semiconductor substrate;

an internal circuit in or on said semiconductor substrate;

a first intra-chip driver or receiver in or on said semiconductor substrate and connected to said internal circuit;

a second intra-chip driver or receiver in or on said semiconductor substrate;

a first metallization structure over said semiconductor substrate;

a passivation layer over said first metallization structure; and

a second metallization structure over said passivation layer, wherein said first and second metallization structures connect ~~structure connects~~ said first intra-chip driver or receiver and said second intra-chip driver or receiver.

123. (previously presented) The circuitry component of Claim 122, wherein said passivation layer comprises a topmost nitride layer of said circuitry component.

124. (previously presented) The circuitry component of Claim 122, wherein said passivation layer comprises a topmost oxide layer of said circuitry component.

125. (previously presented) The circuitry component of Claim 122, wherein said passivation layer comprises a topmost CVD insulating layer of said circuitry component.

Claim 126. (canceled)

127. (previously presented) The circuitry component of Claim 122, wherein said second metallization structure is used to transmit address signals.

128. (previously presented) The circuitry component of Claim 122, wherein said second metallization structure is used to transmit data signals.

129. (previously presented) The circuitry component of Claim 122, wherein said second metallization structure is used to transmit logic signals.

130. (previously presented) The circuitry component of Claim 122, wherein said second metallization structure is used to transmit analog signals.

131. (previously presented) The circuitry component of Claim 122, wherein said second metallization structure is used to transmit clock signals.

132. (previously presented) The circuitry component of Claim 122, wherein said second metallization structure is used to transmit a power voltage.

133. (previously presented) The circuitry component of Claim 122, wherein said second metallization structure is used to transmit a ground voltage.

134. (currently amended) The circuitry component of Claim 122 further comprising an off-chip driver, receiver or I/O circuit in or on said semiconductor substrate, and an external connection~~, wherein said external connection is~~ connected to said off-chip driver, receiver or I/O circuit, ~~and~~ wherein said first and second metallization structures connect ~~structure connects~~ said off-chip driver, receiver or I/O circuit, said first intra-chip driver or receiver, and said second intra-chip driver or receiver.

135. (currently amended) The circuitry component of Claim 134 further comprising an ESD circuit in or on said semiconductor substrate and connected to said external connection.

136. (currently amended) The circuitry component of Claim 122 is a ~~semiconductor~~ chip.

137. (currently amended) The circuitry component of Claim 122 is a ~~semiconductor~~ wafer.

138. (currently amended) The circuitry component of Claim 122, wherein said second metallization structure is used to transmit a power voltage ~~signal~~ output from a voltage regulator.

Claim 139. (canceled)

140. (currently amended) A circuitry component comprising:

a semiconductor substrate;

~~a semiconductor~~ an internal circuit in or on said semiconductor substrate;

an intra-chip driver or receiver in or on said semiconductor substrate and connected to said internal circuit;

an off-chip driver, receiver or I/O circuit in or on said semiconductor substrate;

a first metallization structure over said semiconductor substrate; ~~connecting said semiconductor circuit and said intra-chip driver or receiver;~~

an external connection connected to said off-chip driver, receiver or I/O circuit;

a passivation layer over said first metallization structure; and

a second metallization structure over said passivation layer, wherein said first and second metallization structures connect ~~structure connects~~ said intra-chip driver or receiver and said off-chip driver, receiver or I/O circuit.

141. (previously presented) The circuitry component of Claim 140, wherein said passivation layer comprises a topmost nitride layer of said circuitry component.

142. (previously presented) The circuitry component of Claim 140, wherein said passivation layer comprises a topmost oxide layer of said circuitry component.

143. (previously presented) The circuitry component of Claim 140, wherein said passivation layer comprises a topmost CVD insulating layer of said circuitry component.

Claim 144. (canceled)

145. (previously presented) The circuitry component of Claim 140, wherein said second metallization structure is used to transmit address signals.

146. (previously presented) The circuitry component of Claim 140, wherein said second metallization structure is used to transmit data signals.

147. (previously presented) The circuitry component of Claim 140, wherein said second metallization structure is used to transmit logic signals.

148. (previously presented) The circuitry component of Claim 140, wherein said second metallization structure is used to transmit analog signals.

149. (previously presented) The circuitry component of Claim 140, wherein said second metallization structure is used to transmit clock signals.

150. (previously presented) The circuitry component of Claim 140, wherein said second metallization structure is used to transmit a power voltage.

151. (previously presented) The circuitry component of Claim 140, wherein said second metallization structure is used to transmit a ground voltage.

Claim 152. (canceled)

153. (currently amended) The circuitry component of Claim 140 further comprising an ESD circuit in or on said semiconductor substrate and connected to said external connection.

154. (currently amended) The circuitry component of Claim 140 is a ~~semiconductor~~ chip.

155. (currently amended) The circuitry component of Claim 140 is a ~~semiconductor~~ wafer.

156. (currently amended) The circuitry component of Claim 140, wherein said second metallization structure is used to transmit a power voltage ~~signal~~ output from a voltage regulator.

Claims 157-159. (canceled)

160. (currently amended) A method of fabricating a circuit ~~an electronic~~ component, comprising:

providing a ~~semiconductor~~ wafer comprising a semiconductor substrate, an internal circuit in or on said semiconductor substrate, a first intra-chip driver or receiver in or on said semiconductor substrate and connected to said internal circuit, a second intra-chip driver or receiver in or on said semiconductor substrate, a first metallization structure over said semiconductor substrate, and a passivation layer~~, said passivation layer being~~ over said first metallization structure; and

forming a second metallization structure over said passivation layer, wherein said first and second metallization structures connect ~~interconnecting structure connects~~ said first intra-chip driver or receiver and said second intra-chip driver or receiver.

161. (previously presented) The method of Claim 160, wherein said passivation layer comprises a nitride layer.

162. (previously presented) The method of Claim 160, wherein said passivation layer comprises an oxide layer.

163. (previously presented) The method of Claim 160, wherein said passivation layer comprises an insulating layer formed using a CVD process.

164. (previously presented) The method of Claim 160, wherein said forming said second metallization structure comprises electroplating.

165. (previously presented) The method of Claim 160, wherein said forming said second metallization structure comprises sputtering.

166. (currently amended) A method of fabricating a circuit ~~an electronic~~ component, comprising:

providing a ~~semiconductor~~ wafer comprising a semiconductor substrate, an internal ~~a semiconductor~~ circuit in or on said semiconductor substrate, an intra-chip driver or receiver in or on said semiconductor substrate and connected to said internal circuit, an off-chip

driver, receiver or I/O circuit in or on said semiconductor substrate, a first metallization structure over said semiconductor substrate, an external connection connected to said off-chip driver, receiver or I/O circuit, and a passivation layer over said first metallization structure; ~~, said first metallization structure connecting said intra-chip driver or receiver and said semiconductor circuit, said external connection being connected to said off-chip driver, receiver or I/O circuit, and said passivation layer being over said first metallization structure;~~ and

forming a second metallization structure over said passivation layer, wherein said first and second metallization structures connect ~~structure connects~~ said intra-chip driver or receiver and said off-chip driver, receiver or I/O circuit.

167. (previously presented) The method of Claim 166, wherein said passivation layer comprises a nitride layer.

168. (previously presented) The method of Claim 166, wherein said passivation layer comprises an oxide layer.

169. (previously presented) The method of Claim 166, wherein said passivation layer comprises an insulating layer formed using a CVD process.

170. (previously presented) The method of Claim 166, wherein said forming said second metallization structure comprises electroplating.

171. (previously presented) The method of Claim 166, wherein said forming said second metallization structure comprises sputtering.

172. (new) The circuitry component of Claim 122, wherein said passivation layer comprises a nitride layer having a thickness of greater than 0.4 microns.

173. (new) The circuitry component of Claim 122, wherein said internal circuit has no ESD circuit and no I/O circuit.

174. (new) The circuitry component of Claim 122, wherein said first intra-chip driver or receiver is in series connected to said internal circuit.

175. (new) The circuitry component of Claim 135, wherein said ESD circuit is in parallel connected to said off-chip driver, receiver or I/O circuit.

176. (new) The circuitry component of Claim 122, wherein said second metallization structure comprises an interconnecting line having a thickness of greater than 1 micrometer.

177. (new) The circuitry component of Claim 140, wherein said passivation layer comprises a nitride layer having a thickness of greater than 0.4 microns.

178. (new) The circuitry component of Claim 140, wherein said internal circuit has no ESD circuit and no I/O circuit.

179. (new) The circuitry component of Claim 140, wherein said intra-chip driver or receiver is in series connected to said internal circuit.

180. (new) The circuitry component of Claim 153, wherein said ESD circuit is in parallel connected to said off-chip driver, receiver or I/O circuit.

181. (new) The circuitry component of Claim 140, wherein said second metallization structure comprises an interconnecting line having a thickness of greater than 1 micrometer.

182. (new) The method of Claim 160, wherein said passivation layer comprises a nitride layer having a thickness of greater than 0.4 microns.

183. (new) The method of Claim 160, wherein said internal circuit has no ESD circuit and no I/O circuit.

184. (new) The method of Claim 166, wherein said passivation layer comprises a nitride layer having a thickness of greater than 0.4 microns.

185. (new) The method of Claim 166, wherein said internal circuit has no ESD circuit and no I/O circuit.